AMENDMENTS TO THE SPECIFICATION:

Page 1:

Please change the title to read as follows:

DATA PROCESSOR EMPLOYING REGISTER BANKS WITH OVERFLOW PROTECTION TO ENHANCE INTERRUPT PROCESSING AND TASK SWITCHING

Page 2:

Please substitute the following paragraph for the paragraph beginning at line 23:

The inventor studied a register bank method to ~~shortens~~ shorten interrupt response time. First, an overflow of register banks is taken into account. When an interrupt occurs, some interrupt service routines mask only a critical section having a high ~~emergency~~ priority level such as interrupt factor flag clear with the interrupt level, and after servicing the interrupt, accept re-input of interrupts of the same or lower levels. In such a case where interrupt service is performed by intentionally lowering interrupt levels, since more interrupts than the number of interrupt levels occur, register banks provided by the number of interrupt levels overflows. As a result, a CPU (central

processing unit) taking no measures against overflow may ~~fall into undesirable~~ undesirably stop operation ~~stop~~.

Page 16:

Please substitute the following paragraph for the paragraph beginning at line 23:

The registers to be saved and restored are a predetermined register set whose contents could be destroyed due to interrupts, such as the general purpose registers R0 to R14, the global register GBR, the multiplication registers MACH and MACL, the procedure register PR, and a vector number (IVN) corresponding to a pertinent interrupt as debug information. ~~The~~ Each of the register banks RBK0 to RBKi ~~each are~~ is assigned a storage capacity enough to hold the register set.

Page 17:

Please substitute the following paragraph for the paragraph beginning at line 4:

As for the number of the register banks RBK0 to RBKi, since registers must be saved and restored each time interrupts are nested (interrupts are multiplexed), it is desirable to provide a number of register banks equal, at the minimum, to the number of interrupt levels. If there

are, e.g., 15 interrupt priority levels, 15 register banks RBK0 to RBKi should be provided.

Page 20:

Please substitute the following paragraph for the paragraph beginning at line 22:

FIG. 5 shows how register save processing is performed concurrently with CPU exception handling when an interrupt occurs. Each of registers of the register set is, e.g., 32 bits long. In this case, the dedicated bus 17 for operating the register banks has a width of 128 bits to allow parallel input and output of, e.g., four registers. The wide bus width of the dedicated bus 17 enables concurrent transfer of plural registers and increases transfer efficiency. Since the dedicated bus 17 for operating the register banks is exclusively used for the register banks, the CPU 2 can perform save and restore processing for the register set concurrently with other processing. Register save processing is performed concurrently with CPU exception handling when an interrupt occurs, so that overhead by the register save processing can be apparently zeroed or greatly reduced. In FIG. 5, since saving of the register set is automatically started when an interrupt is accepted, it is started before the first instruction of an interrupt service

routine is fetched according to an interrupt vector, resulting in further increased interrupt ~~responsibility~~responsiveness.